In the Claims

CLAIMS

Claims 1-41 (Canceled).

Claims 42-44 (Canceled).

45. (Previously presented) A method of forming a board on chip package, comprising:

providing an insulative substrate having circuitry thereon and an opening therethrough;

adhering a semiconductive-material-comprising die to the substrate and electrically connecting circuitry supported by the die with the circuitry on the substrate utilizing a plurality of electrical interconnects extending through the opening; and

joining a metal foil to the substrate, the metal foil having segments comprising overlapping portions joined in contact with each other, the segments extending over the die and in physical contact with at least a portion of the die, the metal foil comprising a thickness of less than or equal to about 500 microns.

46. (Original) The method of claim 45 wherein the joining the metal foil to the substrate comprises welding the metal foil to the substrate by melting a portion of the metal foil with a portion of the substrate.

47. (Original) The method of claim 46 wherein the melting is accomplished with a laser.

48. (Original) The method of claim 45 wherein the joining the metal foil to the substrate comprises adhering the metal foil to the substrate with an electrically conductive epoxy.

49. (Original) The method of claim 45 wherein the die has a first surface facing the substrate and a second surface in opposing relation to the first surface, the foil being in physical contact with only a portion of said second surface.

Claim 50 (Canceled).

51. (Original) The method of claim 45 wherein the die has a first surface facing the substrate, a second surface in opposing relation to the first surface, and a sidewall between the first and second surfaces, the foil being joined to the substrate proximate the sidewall and extending across the sidewall to physically contact the second surface.

52. (Original) The method of claim 51 wherein the sidewall has a length, and wherein the foil physically contacts a predominate portion of the sidewall length.

Claims 53-54 (Canceled).

55. (Original) The method of claim 45 wherein the metal foil is selected from the group consisting of copper foil and aluminum foil.

56. (Original) The method of claim 45 further comprising adhering the die to the substrate with an electrically conductive epoxy.

57. (Currently amended) A method of forming a board on chip package, comprising:

providing an insulative substrate having circuitry thereon and an opening therethrough, the substrate having a pair of opposing surfaces, the surfaces being a first surface and a second surface, the circuitry being on the first surface;

adhering a metal foil to the second surface;

adhering a semiconductive-material-comprising die to the metal foil and substrate, the die having circuitry supported thereby and comprising sidewalls extending from the insulative substrate, the metal foil physically contacting at least a portion of at least one sidewall; ~~and~~

electrically connecting the circuitry supported by the die to the circuitry on the substrate with a plurality of electrical interconnects extending through the opening; and

wherein the die has a pair of opposing sides; wherein the die covers a portion of the metal foil and leaves an other portion of the metal foil extending outwardly beyond one of the opposing sides of the die; and further comprising wrapping at least some of said other portion of the foil along the at least one of the opposing sides of the die.

Claims 58 (Canceled).

59. (Currently amended) The method of claim ~~58~~ 57 wherein the die comprises a first surface facing the substrate and second surface in opposed relation to the first surface, the other portion of the foil being wrapped along both of the opposing sides of the die and over the second surface of the die.

Claims 60-62 (Canceled).

63. (Original) A method of forming a board on chip package, comprising: providing an insulative substrate having circuitry thereon and an opening therethrough, the substrate comprising a first surface and a second surface in opposing relation to the first surface, the circuitry being on the first surface, the substrate further comprising a cavity extending into the second surface and proximate the opening;

placing a semiconductive-material-comprising die within the cavity and electrically connecting circuitry supported by the die to the circuitry on the substrate first surface with a plurality of conductive interconnects extending through the opening, the die having an inner surface facing the substrate and an outer surface in opposing relation to the inner surface; and

placing a metal sheet outwardly of the die and in physical contact with at least a portion of the die outer surface.

64. (Original) The method of claim 63 wherein the die has a portion extending outwardly of the cavity, and wherein the sheet extends along the second surface of the substrate and over the portion of the die extending outwardly of the cavity, the method further comprising bonding the sheet to the second surface of the substrate.

65. (Original) The method of claim 63 wherein the die is entirely received in the cavity inwardly of the second surface of the substrate, and wherein the sheet extends along the second surface of the substrate and over the cavity to enclose the die in the cavity, the method further comprising bonding the sheet to the second surface of the substrate.

66. (Original) The method of claim 63 wherein the metal sheet is selected from the group consisting of copper foil and aluminum foil.

67. (Original) The method of claim 63 further comprising adhering the die to the substrate with an electrically conductive epoxy.

68. (Original) A method of forming a plurality of board on chip packages, comprising:

providing an insulative substrate having a repeating circuitry pattern thereon and a plurality of openings therethrough, the openings being in one-to-one correspondence with individual of the repeated circuitry patterns;

adhering a plurality of semiconductive-material-comprising dies to the substrate and electrically connecting circuitry supported by the dies with the circuitry on the substrate utilizing a plurality of electrical interconnects extending through the openings;

joining a metal foil to the substrate and extending the metal foil over the plurality of dies; and

cutting the substrate and metal foil to form singulated die packages comprising a single die, a portion of the substrate having a single repeated pattern of the circuitry, and a portion of the metal foil.

69. (Original) The method of claim 68 wherein the substrate comprises areas between the die, and wherein the metal foil is bonded to such areas before the cutting of the substrate.

70. (Original) The method of claim 69 wherein the bonding comprises welding the metal foil to the substrate by melting a portion of the metal foil and a portion of the substrate.

71. (Original) The method of claim 69 wherein the bonding comprises adhering the metal foil to the substrate with an adhesive.

72. (Original) The method of claim 69 wherein the bonding comprises adhering the metal foil to the substrate with an electrically conductive adhesive.

73. (Original) The method of claim 69 wherein the bonding comprises adhering the metal foil to the substrate with silver-filled epoxy.

74. (Original) The method of claim 68 wherein the substrate comprises areas between the die, and wherein the metal foil is not bonded to said areas until during or after the cutting of the substrate.

75. (Previously presented) A method of forming a board on chip package, comprising:

providing an insulative substrate having circuitry thereon and an opening therethrough, the substrate having a pair of opposing surfaces, the surfaces being a first surface and a second surface, the circuitry being on the first surface;

adhering a metal foil to the second surface;

adhering a semiconductive-material-comprising die to the metal foil, the die having circuitry supported thereby;

electrically connecting the circuitry supported by the die to the circuitry on the substrate with a plurality of electrical interconnects extending through the opening; and

wherein the die has a pair of opposing sides; wherein the die covers a portion of the metal foil and leaves an other portion of the metal foil extending outwardly beyond one of the opposing sides of the die; and further comprising wrapping at least some of said other portion of the foil along the at least one of the opposing sides of the die.

76. (Previously presented) The method of claim 75 wherein the die comprises a first surface facing the substrate and second surface in opposed relation to the first surface, the other portion of the foil being wrapped along both of the opposing sides of the die and over the second surface of the die.

77. (Previously presented) A method of forming a board on chip package, comprising:

providing an insulative substrate having circuitry thereon and an opening therethrough, the substrate having a pair of opposing surfaces, the surfaces being a first surface and a second surface, the circuitry being on the first surface;

adhering a metal foil to the second surface;

adhering a semiconductive-material-comprising die to the metal foil, the die having circuitry supported thereby;

electrically connecting the circuitry supported by the die to the circuitry on the substrate with a plurality of electrical interconnects extending through the opening; and

wherein the die has a pair of opposing sides; wherein the die covers a portion of the metal foil and leaves a pair of other portions of the metal foil extending outwardly beyond the opposing sides of the die; said pair of other portions comprising a first other portion which extends outwardly of the first side of the die, and a second other portion which extends outwardly of the second side of the die; the method further comprising wrapping the first other portion of the foil along the first of the opposing sides of the die, and wrapping the second other portion of the foil along the second of the opposing sides of the die.

78. (Previously presented) The method of claim 77 wherein die comprises a first surface facing the substrate and second surface in opposed relation to the first surface, the first and second other portions of the foil joining one another over the second surface of the die.

79. (Previously presented) The method of claim 78 wherein the first and second other portions overlap one another over the second surface of the die.

80. (New) A method of forming a board on chip package, comprising:

providing an insulative substrate having circuitry thereon and an opening therethrough, the substrate having a pair of opposing surfaces, the surfaces being a first surface and a second surface, the circuitry being on the first surface;

adhering a metal foil to the second surface;

adhering a semiconductive-material-comprising die to the metal foil and substrate, the die having circuitry supported thereby and comprising sidewalls extending from the insulative substrate, the metal foil physically contacting at least a portion of at least one sidewall;

electrically connecting the circuitry supported by the die to the circuitry on the substrate with a plurality of electrical interconnects extending through the opening; and

wherein the die has a pair of opposing sides; wherein the die covers a portion of the metal foil and leaves a pair of other portions of the metal foil extending outwardly beyond the opposing sides of the die; said pair of other portions comprising a first other portion which extends outwardly of the first side of the die, and a second other portion which extends outwardly of the second side of the die; the method further comprising wrapping the first other portion of the foil along the first of the opposing sides of the die, and wrapping the second other portion of the foil along the second of the opposing sides of the die.

81. (New) The method of claim 80 wherein die comprises a first surface facing the substrate and second surface in opposed relation to the first surface, the first and second other portions of the foil joining one another over the second surface of the die.

82. (New) The method of claim 81 wherein the first and second other portions overlap one another over the second surface of the die.